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*Inventors: Jayesh R. Bhakta et al.*

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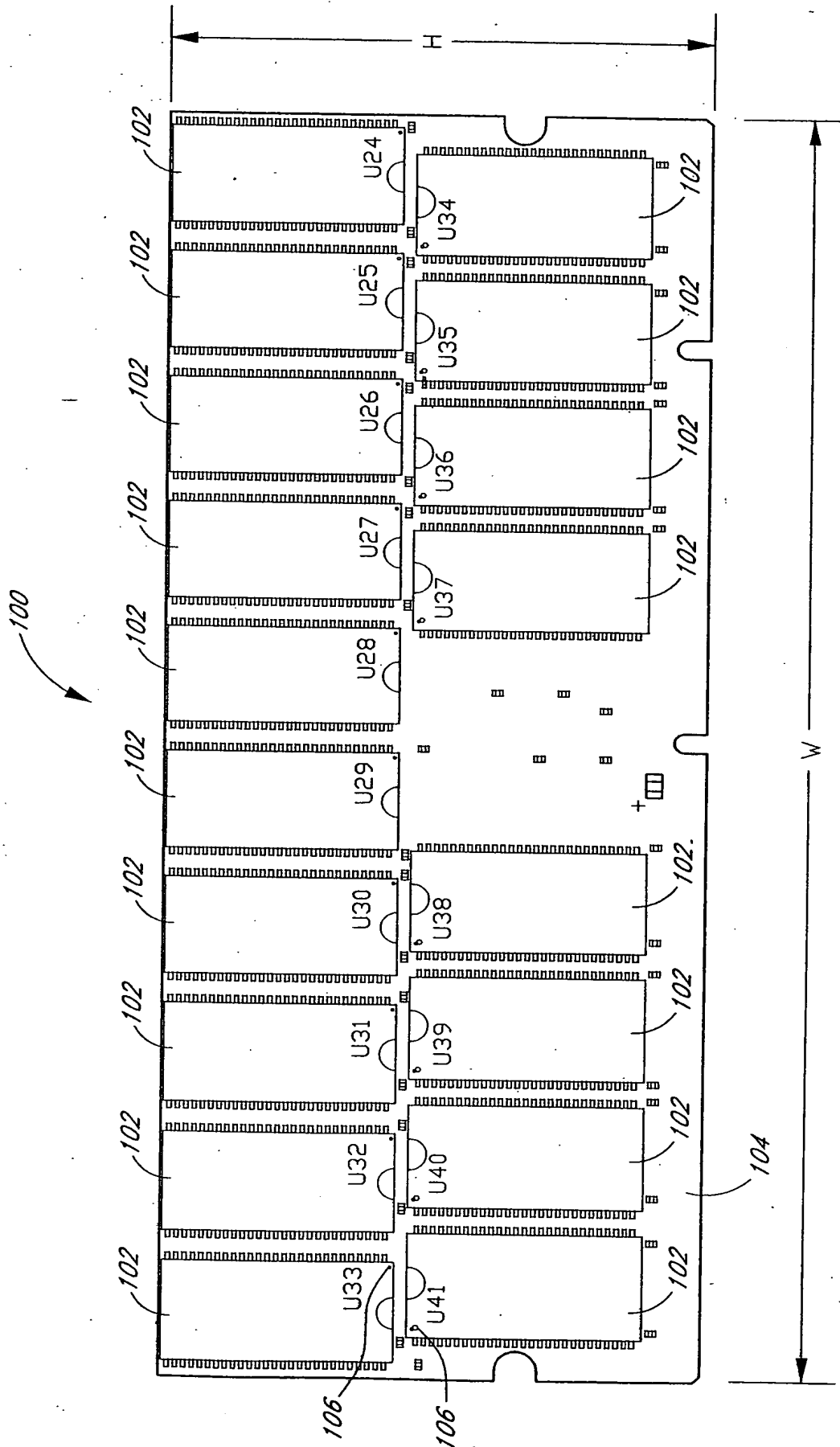


FIG. 1B

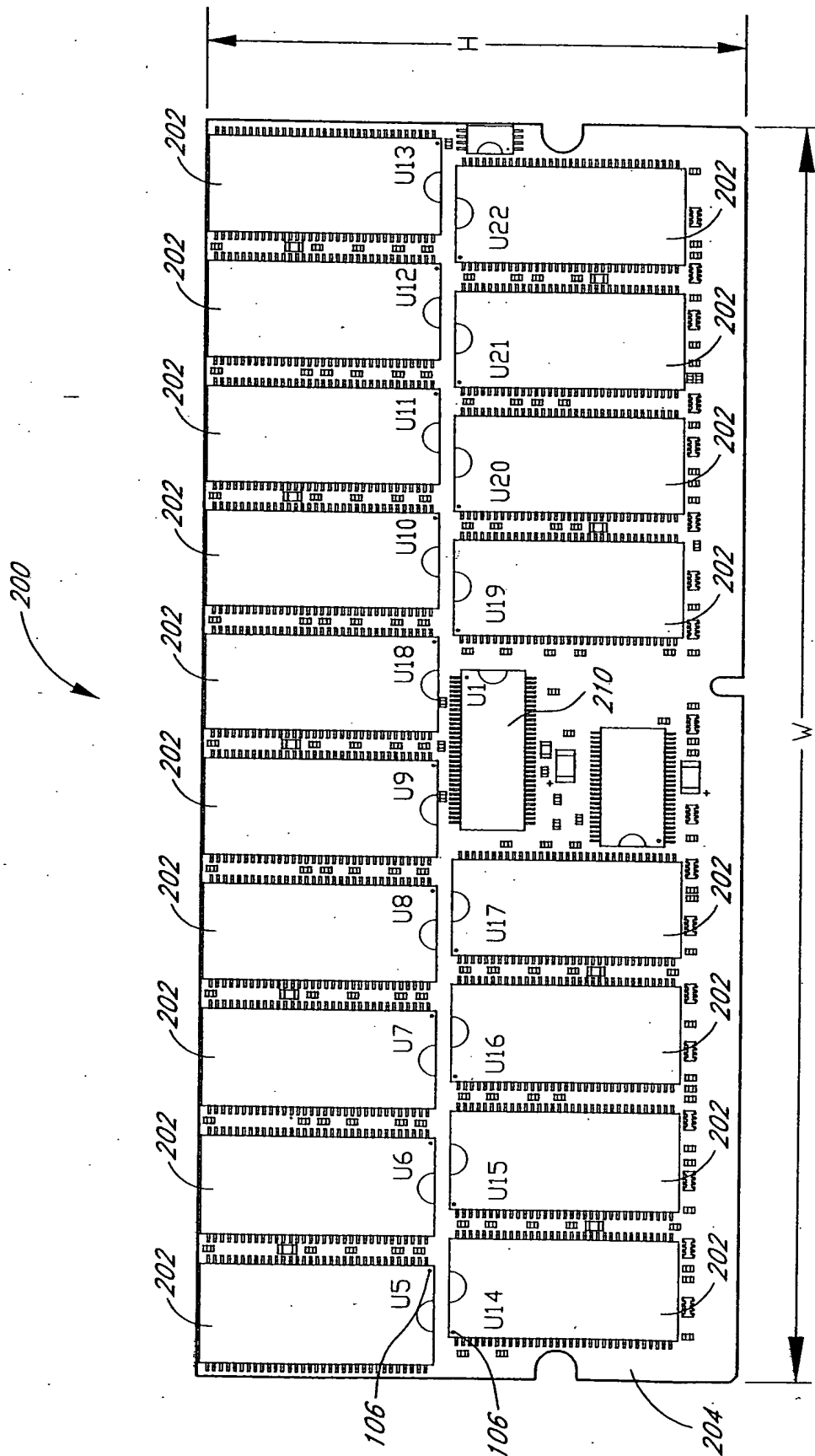


FIG. 2A

ARRANGEMENT OF INTEGRATED CIRCUITS  
IN A MEMORY MODULE  
Inventors: Jayesh R. Bhakta et al.  
Filed: January 30, 2004 Atty Docket: NETL.001C1  
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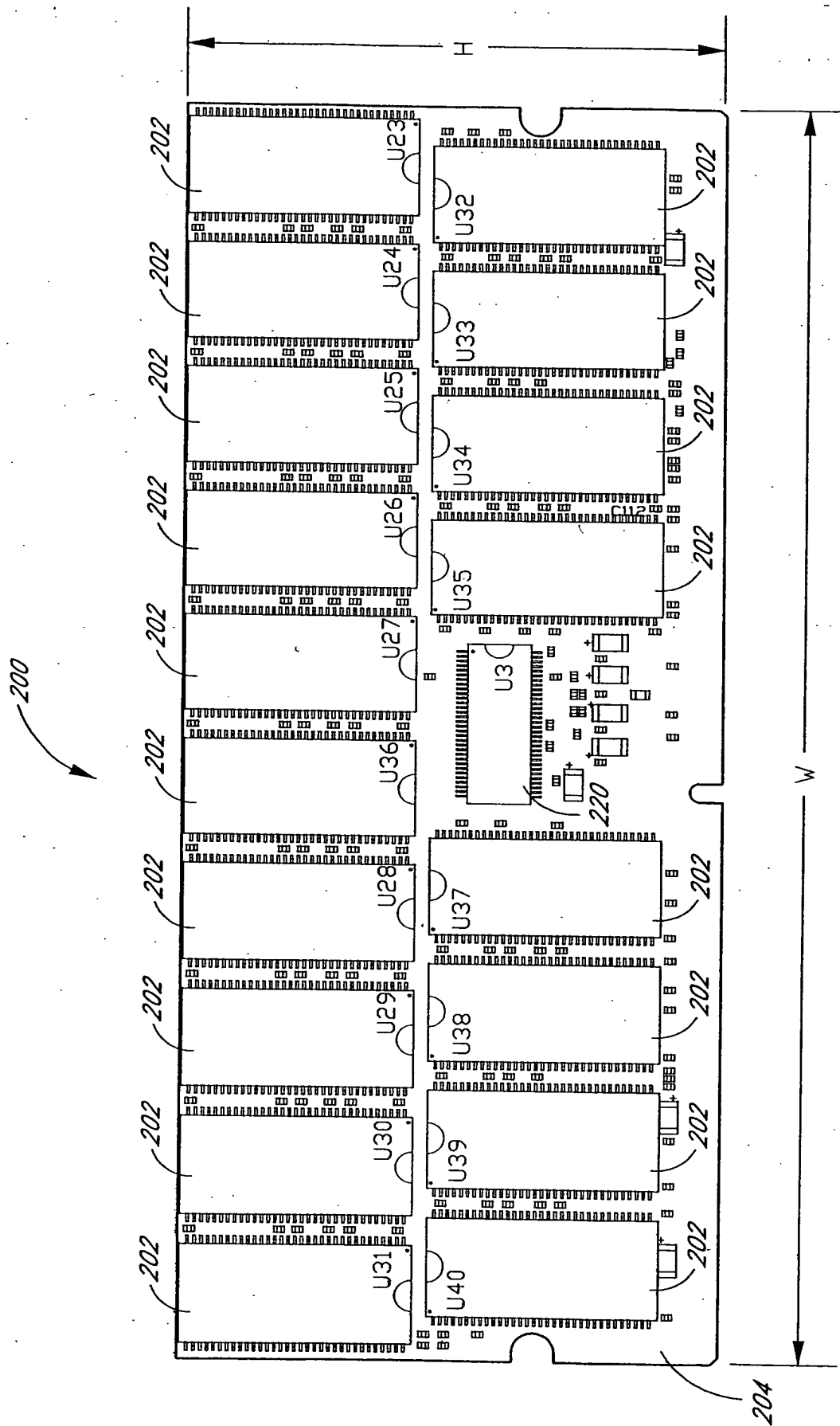


FIG. 2B

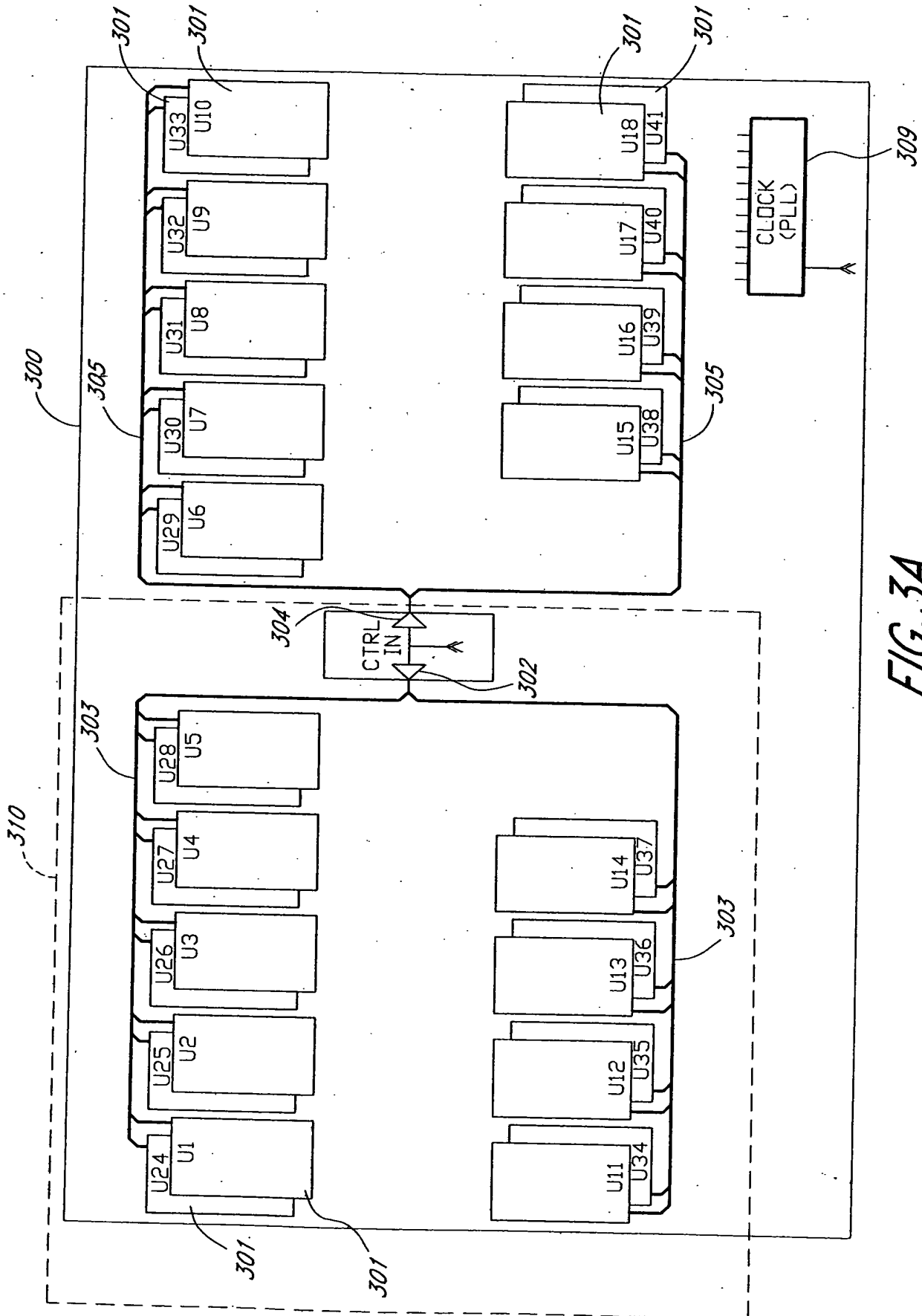


FIG. 3A

ARRANGEMENT OF INTEGRATED CIRCUITS  
IN A MEMORY MODULE

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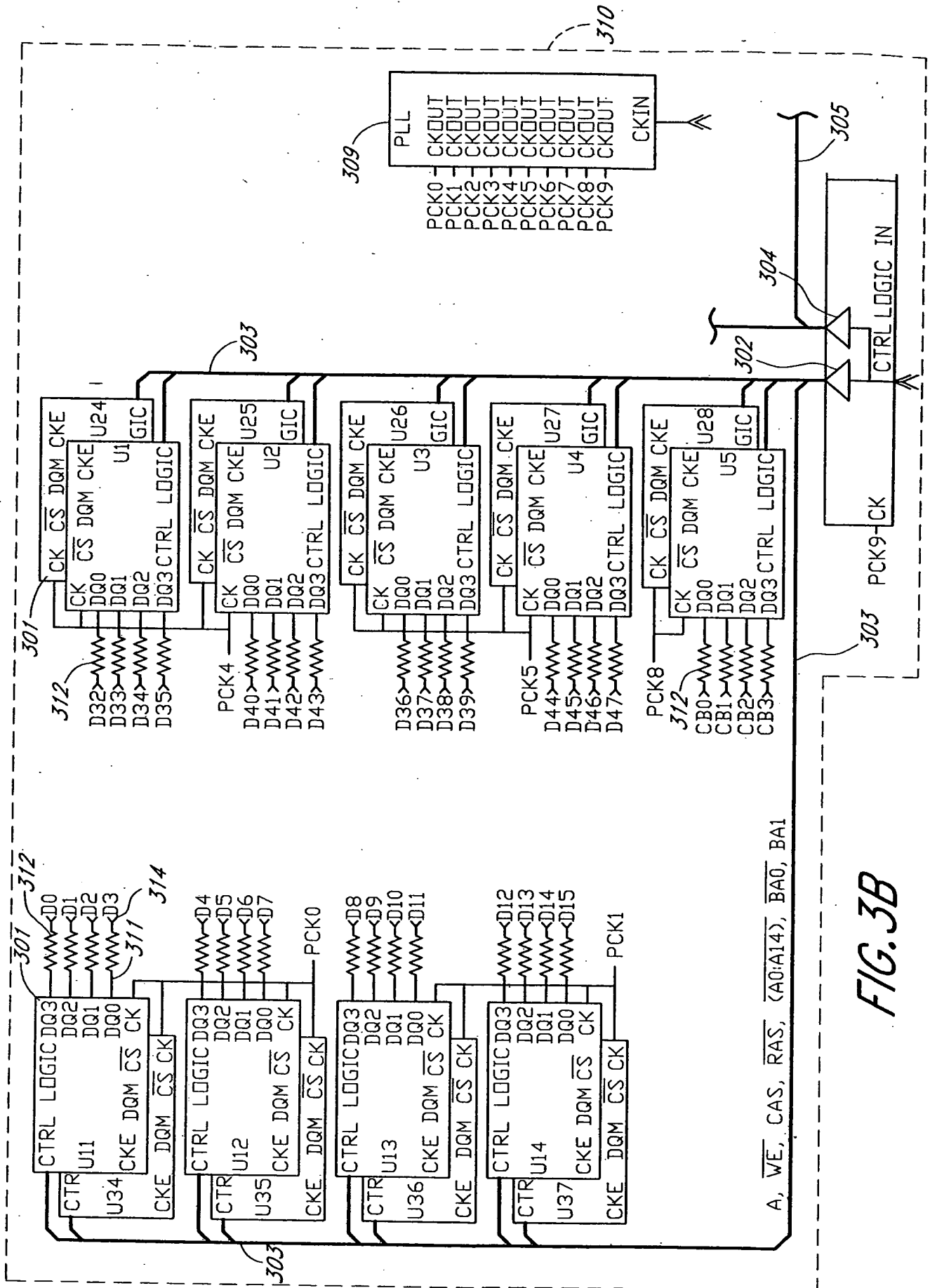


FIG. 3B

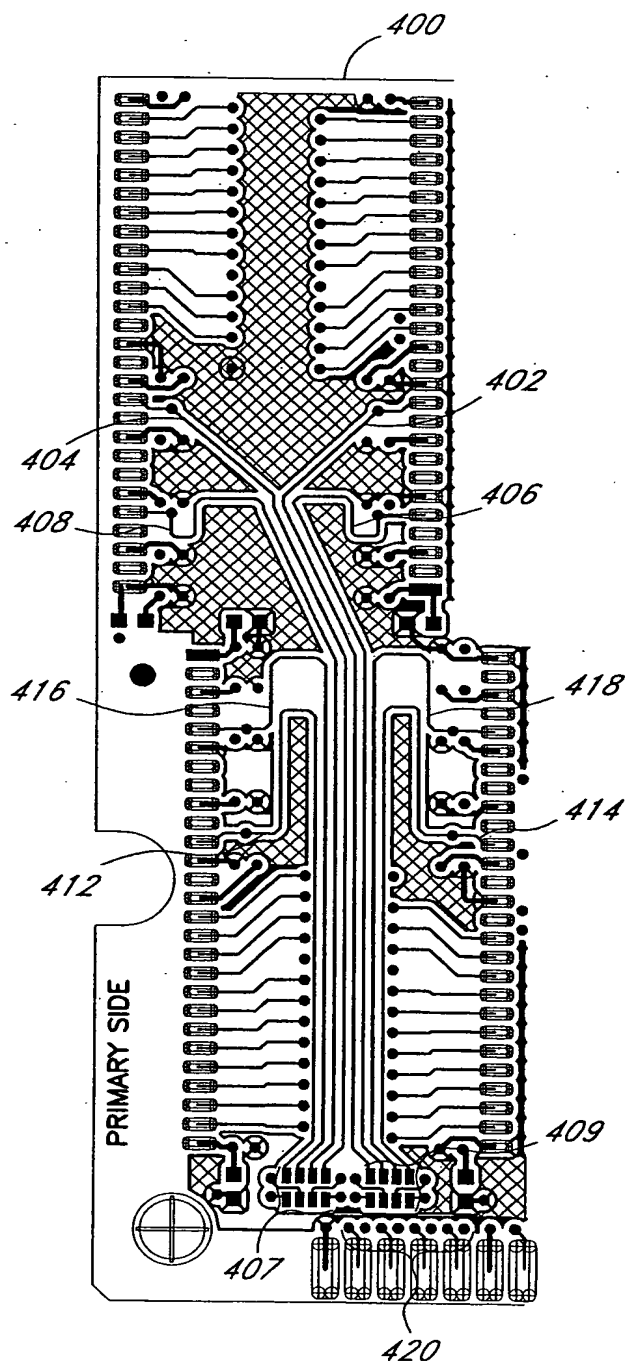


FIG. 4A



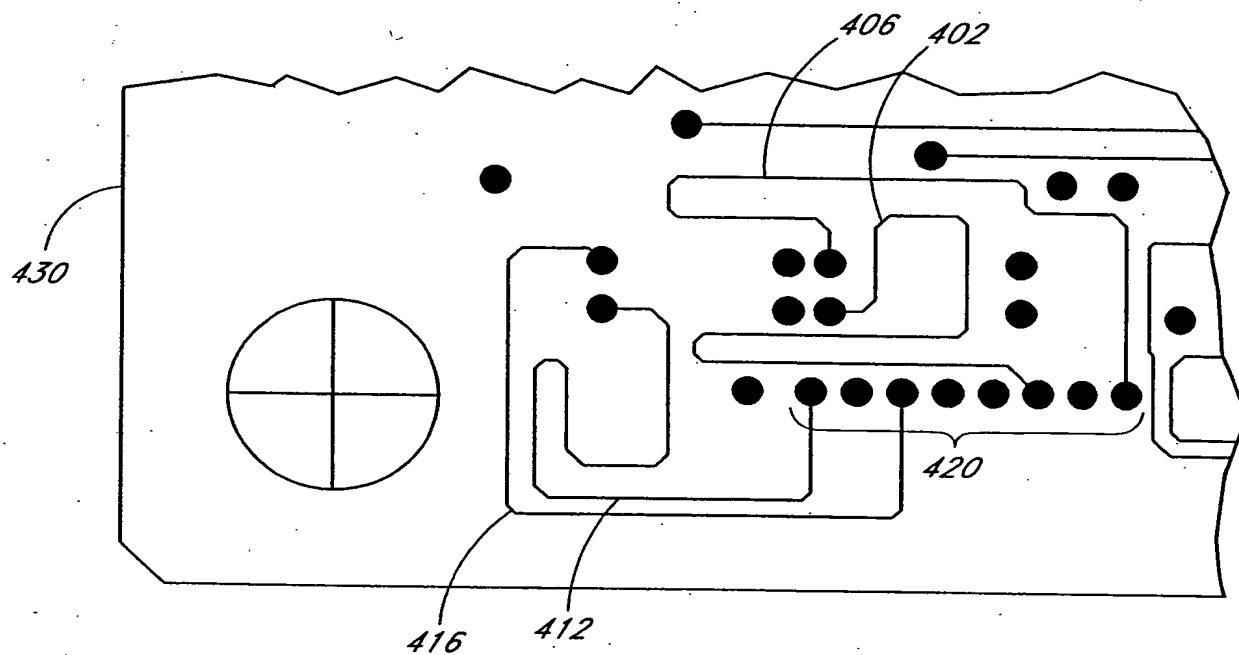


FIG. 4B

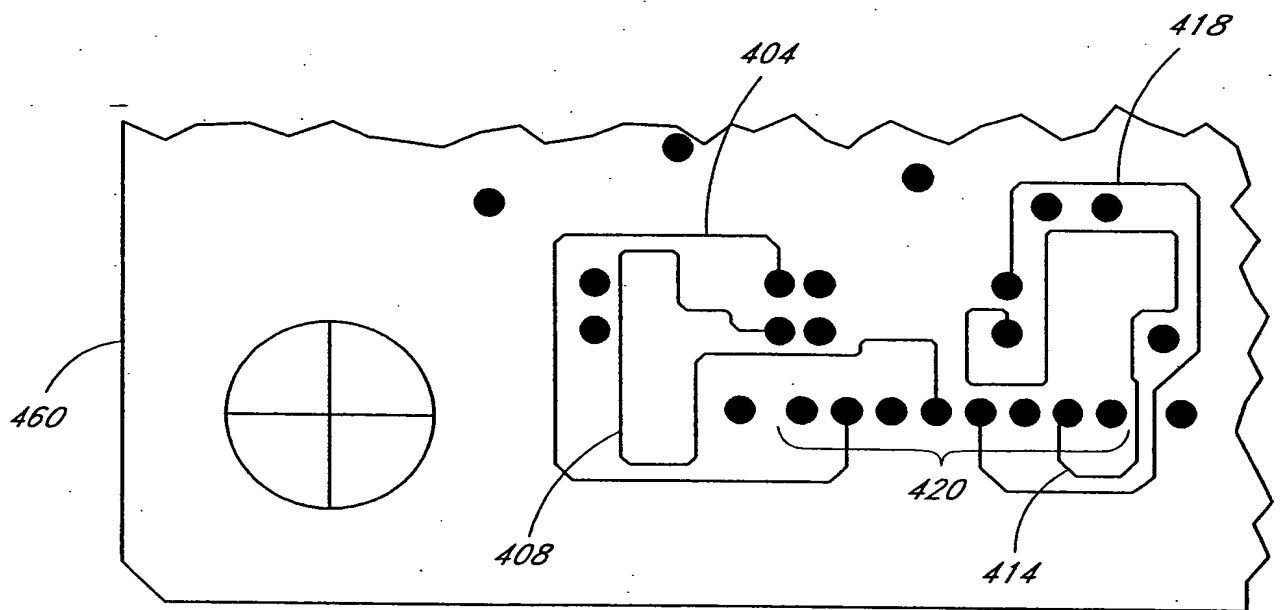


FIG. 4C